ABSTRACT OF THE INVENTION

An output buffer includes a first drive circuit that receives an input signal having a sharp waveform and generates an output signal that has a gentle waveform. A second drive circuit is connected to the first drive circuit at an output terminal and has a lower impedance than the first drive circuit. A delay circuit is also connected to the output terminal and generates a delayed output signal. A first control circuit is connected between the delay circuit and the second drive circuit and receives the input signal and the delayed output signal and generates a first control signal used to drive the second drive circuit.